Nick Collins
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Currently based near Chandler, AZ

Expertise Summary:

- System Verilog OVM/UVM
- Requirement extraction and Testplan creation
- Test environment creation and upgrades
- Seq/Test writing and debug
- Coverage coding, closure and exclusions
- VCS/Verdi, Mentor and Cadence simulators
- Gate-level simulation (GLS)

Experience:

Intel Corp – Jan '21 to Apr '24 Chandler, AZ

As **Senior Verification Engineer**, developed UVM stimulus, coverage and checks for new features for Intel's latest Infrastructure Processing Unit (IPU), aka Smart NIC. As verification lead, also assigned priority for multitude of tasks in order to meet milestones. Responded to SoC and cluster support requests as our IP was integrated at higher levels. Responsible for IP verification documentation. Analyzed and pushed functional coverage using HVP. Wrote seqs/tests and debugged simulation failures. Top-level interfaces included AXI-streaming and APB.

FirstPass Engineering – Feb '18 to Aug '20 Phoenix, AZ

As a **consulting engineer**, created block-level testplan for List Processing Engine (LPE), which was part of a switch/router core ASIC. Also created UVM test environment with custom-built UVM agents that able to be vertically re-usable for chip-level testing. Wrote checks in UVM Scoreboard/model and cover groups/points as per testplan. Worked with designer to close structural and functional coverage.

As a **consulting engineer**, contributed to sequence and test writing for satellite ASIC with APB and SPI interfaces. Tasks included register testing, coverage writing and assertions. Customized SPI agent for block and chip-level test benches. Debugged nightly regression failures as needed.

Waymo/Google (via Adecco) – Aug '17 to Nov '17 Mountain View, CA

As a **consulting engineer**, created UVM testbench from scratch to verify AXI networking IP. Leveraged existing AXI UVM VIP to create configurable multi-master/slave environment that would be easily scalable to any number of agents as DUT changed. Created self-checking UVM Scoreboard to check data and to predict/check slave targets given master addresses. Also coded virtual sequences to simulate multi-master simultaneous transactions.

FirstPass Engineering – Oct '14 to June '17 Chandler, AZ

As a **consulting engineer**, debugged regression failures in VERA environment for Gen3 RapidIO-based design. Also created new testcases to meet top-level coverage goals.

As a **consulting engineer**, integrated Ethernet compliance tests into UVM test environment. This involved new base test, RAL integration and coding sequence self-checking as per compliance requirements.

As a **consulting engineer**, created, maintained and debugged OVM environment for packet scheduler IP (part of larger NIC), specifically rate limiter block. Developed testplan: checks and coverage. Executed testplan including OVM scoreboards and functional coverage. Test and sequence writing/debug.

Intel Corp – June ‘10 to April ‘14 Chandler, AZ

As **Senior Verification Engineer**, created OVM-based test sequences for USB IP. Wrote OVM classes describing USB EHCI data structures. Responsible for integrating new releases of sub IP’s. Integration involved stitching RTL and debugging sims until regressions stabilized.

Served as project lead on two other security-related IP's. This involved running execution meetings, dividing tasks, making priority calls for customer needs and also filling in technically for verification-related tasks, as needed. Also performed testplan extraction, coding seqs, GLS, coding covergroups for functional coverage, coding/maintaining OVM agents/scoreboard and preparing for verification reuse for higher integration.

Intel Corp – Feb ‘08 to April `10 Chandler, AZ

As a **consulting engineer**, provided verification services for developing SoC with embedded Intel processor. Worked in System Verilog AVM environment writing sims for Intel DFT logic and for Clock/Reset logic of SoC. Also helped in verifying CPU-related sims with Intel cosimulation tool (DVT) to communicate between VCS and ModelSim simulators. Also, initiated conversion flow of SoC RTL cosimulation from mixed-sim to entirely VCS.

As a consulting engineer, designed re-usable DFx IP RTL using System Verilog. Generated and executed Testplan for verifying RTL using System Verilog OVM. Created and maintained OVM environment for DFx designs. Employed constrained-random stimulus to maximize functional coverage results. Generated functional coverage and code coverage reports using VCS.

Qualcomm Inc – Sep ‘07 to Jan ‘08 Chandler, AZ

As a **consulting engineer**, provided design and verification services on mixed-signal power management IC. Designed RTL for OTP memory controller with SPI interface. Created verilog models for analog portions of design from Cadence schematics and designer feedback. Wrote testbench using System Verilog and debugged top-level sims using VCS.

Intel Corp -- Oct ‘05 to Apr ‘06 Chandler, AZ

As a **consulting engineer,** provided verification services for developing a Network Processor SoC. Primarily focused on Gigabit Ethernet controller performing RTL and gate-level simulations. Performed code coverage using VNavigator and MTI. Responsible for identifying and resolving various bugs found in the design and testbench. Created random simcases which performed exhaustive testing and was also leveraged for functional coverage. Also verified separate unit performing RGMII translation.

Canesta Inc – Feb ‘05 to May ‘05 Sunnyvale, CA

As a **consulting engineer**, provided design and verification services for 3D-imaging ASIC using VHDL with ModelSim simulator. Designed RTL for SPI, DMA interface and other internal sub-designs. Created verification infrastructure for block-level and top-level sims using VHDL and C-shell scripts. Wrote Perl scripts to generate random data for RAM simulations in VHDL. Debugged gate-level netlist and SDF problems in GLS.

Intel Corp -- Aug ‘03 to Aug ‘04 Chandler, AZ

As a **consulting engineer**, provided verification services for developing a 1.2M AFE-Baseband SoC design. Designed baseband signaling and bus interface block. Contributed to full-chip integration. Developed self-checking, block-level and top-level Verilog sim cases. Modularized common testbench interfaces into transactors (BFMs) that can be re-used in higher-level sims. Created scripts for simulation regressions using MTI and VCS simulators. Generated EVCD vectors for IMS lab testing.

Bandspeed Inc -- July ‘02 to Dec ‘02 Austin, TX

As a **consulting engineer**, provided verification services for developing an Ethernet switch design. Developed Verilog functional models for the external Ethernet MII interface. Also, created internal bus interface models for block-level simulations. These Verilog models included self-checking tasks/functions to simplify simcase writing. Responsible for writing and debugging dozens of block-level sims for two major blocks.

Intel Corp -- Oct '98 to Oct '01 Sacramento, CA

As a **consulting engineer**, developed VHDL and Verilog test environments for serial controller coded in VHDL. Test environment included memory, test cases, procedures, and pad module. Also helped to integrate the serial controller design into another ASIC.

As a **consulting engineer**, integrated IP switch core with eight 10/100 PHYs for an 8-port Ethernet switch ASIC. This involved pad instantiation, testmode configuration, and pin multiplexing. Worked closely with synthesis team.

As a **consulting engineer**, used MTI simulator and developed VHDL sims for verifying multiport Ethernet 10/100 transceiver. Most simulations written specifically for RMII interface of ASIC, such as RX and TX of packets, FIFO operation, and out-of-band signaling.

As a **consulting engineer,** provided verification services for developing a Gigabit PHY core. Helped integrate this PHY into a four-port Gigabit Ethernet transceiver ASIC and also participated in its RTL verification. Responsible for writing and debugging many top-level sims in Verilog. Wrote Verilog behavioral models for analog portions for simulation purposes.

Lockheed Martin -- June '96 to Aug '98 Sunnyvale, CA

Served as **ASIC Design/Verif Engineer** on 72k-gate, radiation-hard, attitude control and telemetry interface ASIC. Coded design in VHDL and simulated using VSS. Synthesized design using Synopsys. Inserted internal scan chains and created ATPG vectors. Performed static-timing analyses using DesignTime. Performed gate-level verification by vector comparison. Used QuickTurn emulator to debug board/ASIC issues prior to tape-out.

Academic Background:

Louisiana State University: BSEE, June 1996.